In the Specification:

Please replace paragraph **[0019]** with the following paragraph:

-- **[0019]** Referring to Figure 6, a copper barrier layer 33 (e.g., the nitride layer 33) having a high dielectric constant k is successively deposited in a thin thickness of about ~~100 to 500~~ 50 to 200 Å on the insulating layer 11 and on the CuN layer 31 without time delay, while leaving the semiconductor substrate 10 as it is.--.

Please replace paragraph **[0020]** with the following paragraph:

-- **[0020]** As shown in Figure 5, since the copper barrier layer 31 has already been formed on the copper layer 15, a thinner nitride layer 33 can be deposited as compared to the nitride layer 33 required in the conventional process. The use of this thinner nitride layer 33 prevents degradation of the ~~operational velocity~~ operating speed of the semiconductor device due to an increase of the dielectric constant between the insulating layers.--.

Please replace paragraph **[0024]** with the following paragraph:

-- **[0024]** The stability of the process for removing the CuO layer 16 is secured and a contact characteristic of the semiconductor device is improved by performing plasma processing using NH3 or N2 gas with little explosive possibility, instead of performing a conventional plasma processing using

explosive H2 gas to remove the CuO layer 16 that is parasitically formed on the copper layer 15. Furthermore, a high dielectric constant nitride layer 33 is thinly formed on the copper layer 15 to thereby increase the ~~operational velocity~~ operating speed of the semiconductor device, by forming the CuN layer 31 on the copper layer 15 while removing the CuO layer 16.--.

Please replace paragraph **[0026]** with the following paragraph:

-- **[0026]** As described above, the illustrated method of manufacturing semiconductor devices is performed using a Damascene process. The contact hole 12 of the insulating layer 11 is filled with the copper layer 15 and, then, the copper layer 15 is planarized. During the planarizing, the CuO layer 16 is parasitically formed on the surface of the copper layer 15. The CuO layer 16 is removed by plasma processing using ammonia or nitrogen. The conductive CuN layer 31, (i.e., the copper barrier layer), is formed on the surface of the copper layer 15. The nitride layer 33, (i.e., the copper barrier layer for the copper layer), is deposited on the insulating layer 11 and the CuN layer 31. Then, the upper insulating layer 35 is deposited on the nitride layer 33, and the upper contact hole 36 is formed in the upper insulating layer 35 and the nitride layer 33 to expose the copper layer 15. Then, the upper contact ~~hole36~~ hole 36 is filled with the upper copper layer 39 and the upper copper layer 39 is planarized.--.

Please replace paragraph **[0029]** with the following paragraph:

-- **[0029]** A disclosed method of manufacturing a semiconductor ~~devicecomprises~~ device comprises: forming a contact hole 12 in an insulating ~~layer11~~ layer 11; filling the contact hole 12 with a copper layer 15; planarizing the copper layer 15; removing a copper oxide layer 16 parasitically formed on the surface of the copper layer 15; depositing a copper barrier layer 33 on the insulating layer 11 and the copper layer 15; depositing an upper insulating layer 35 on the copper barrier layer 33; and forming an upper contact hole in the copper barrier layer 33 and the upper insulating layer 35 so as to expose the copper layer15.--.